AMENDMENTS TO THE CLAIMS

The listing of claims below replaces all prior versions of claims in the application.

1. – 12. (Cancelled)

13. (Previously Presented) A scrambling code generation apparatus generating a scrambling code used in a scrambling operation of transmission data, comprising:

a shift register formed of a plurality of stages of registers connected so as to execute a feedback operation and a spreading operation to generate a sequence of scrambling codes by a predetermined generating polynomial;

an arithmetic circuit computing values of said registers involved with said feedback operation and said spreading operation that would have been obtained if said shift register carries out a shift operation for an increasing predetermined number of times based on predetermined initial values;

an input circuit applying said computed values of registers into corresponding said registers; and

a control circuit controlling said arithmetic circuit and said input circuit so that said arithmetic circuit computes values of said registers and said input circuit applies said computed values into said registers until all said plurality of stages of registers store valid values based on said computed values and said input values;

wherein said shift register continues a shift operation based on valid values stored in all of said plurality of stages of registers to generate said sequence of scrambling codes.

14. (Original) The scrambling code generation apparatus according to claim 13, further comprising:

a storage circuit storing said predetermined initial values; and

a matrix supply circuit supplying a matrix to determine values of registers involved with said feedback operation and said spreading operation after shift operations of said increasing predetermined number of times based on said predetermined generating polynomial,

wherein said arithmetic circuit multiplies said predetermined initial values stored in said storage circuit by said matrix supplied from said matrix supply circuit to compute values of said registers.

15. (Original) The scrambling code generation apparatus according to claim 13, further comprising a storage circuit storing said predetermined initial values,

wherein said arithmetic circuit obtains by a predetermined operation a matrix to determine values of registers involved with said feedback operation and said spreading operation after shift operations of said increasing predetermined number of times based on said predetermined generating polynomial, and multiplying by said predetermined initial values stored in said storage means to compute values of said registers.

16. (Cancelled)

17. (Previously Presented) A portable radio terminal of digital radio communication, comprising:

a transmission related modem modulating transmission data; and

a radio processor applying processing for radio communication on transmission data of said transmission related modem to send out the processed data as a transmission radio signal;

said transmission related modem comprising a scrambling code generation apparatus generating a scrambling code used in a scrambling operation of said transmission data,

said scrambling code generation apparatus comprising:

a shift register formed of a plurality of stages of registers connected so as to execute a feedback operation and a spreading operation to generate a sequence of scrambling codes by a predetermined generating polynomial;

an arithmetic circuit computing values of said registers involved with said feedback operation and said spreading operation that would have been obtained if said shift register carries out a shift operation for an increasing predetermined number of times based on predetermined initial values;

an input circuit applying said computed values of registers into corresponding said registers; and

a control circuit controlling said arithmetic circuit and said input circuit so that said arithmetic circuit computes values of said registers and said input circuit applies said computed

values into said registers until all said plurality of stages of registers store valid values based on said computed values and said input values;

wherein said shift register continues a shift operation based on valid values stored in all of said plurality of stages of registers to generate said sequence of scrambling codes.

18. (Original) The portable radio terminal according to claim 17, further comprising:

a storage circuit storing said predetermined initial values; and

a matrix supply circuit supplying a matrix to determine values of registers involved with said feedback operation and said spreading operation after shift operations of said increasing predetermined number of times based on said predetermined generating polynomial,

wherein said arithmetic circuit multiplies said predetermined initial values stored in said storage circuit by said matrix supplied from said matrix supply circuit to compute values of said registers.

19. (Original) The portable radio terminal according to claim 17, further comprising a storage circuit storing said predetermined initial values,

wherein said arithmetic circuit obtains by a predetermined operation a matrix to determine values of registers involved with said feedback operation and said spreading operation after shift operations of said increasing predetermined number of times based on said predetermined generating polynomial, and multiplying by said predetermined initial values stored in said storage means to compute values of said registers.

20. (Cancelled)